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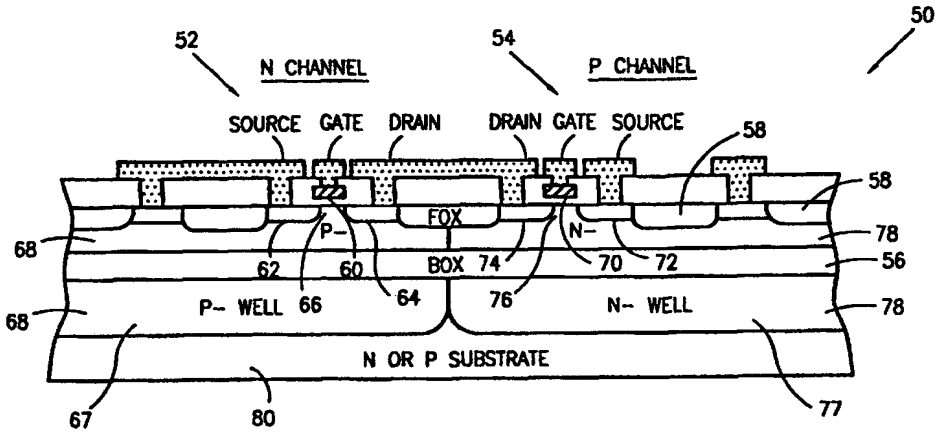

(57) Abstract

A method for creating a SOI CMOS type device compatible with bulk CMOS using a bulk CMOS physical layout database. The method uses the P–well and N–well masks used in fabrication of bulk CMOS devices. The N–well and P–well regions are fabricated by implanting the appropriate dopants above and below the buried oxide layer to create the basic SOI CMOS structure. Particular modifications to the basic SOI CMOS structure include providing a mask for establishing ohmic contact with the wells below the buried oxide layer. The modification uses a separate mask which is generated from the existing bulk CMOS mask database. The mask is generated by doing the following logical AND and OR functions on the existing CMOS layers: a) SOURCE/DRAIN [AND] P^+ [AND] P–WELL [AND] 1st CONTACT; b) SOURCE/DRAIN [AND] N^+ [AND] N–WELL [AND] 1st CONTACT; c) a) [OR] b).

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SILICON-ON-INSULATOR CONFIGURATION WHICH IS COMPATIBLE WITH BULK CMOS ARCHITECTURE

TECHNICAL FIELD

The present invention relates to semiconductor device configurations and manufacturing processes. In particular, the invention relates to a silicon-on-insulator (SOI) configuration and manufacturing process which is compatible with existing bulk complementary metal oxide semiconductor (CMOS) device architectures.

BACKGROUND OF THE INVENTION

Complementary metal oxide semiconductor (CMOS) devices that are produced in mass quantities are referred to as "bulk" CMOS, because they include a semiconductive bulk substrate on which active or passive circuit elements are disposed. Recently, silicon-on-insulator (also referred to as silicon-oxide-insulator) SOI CMOS devices have been introduced which consume less power than do bulk CMOS devices. SOI devices are characterized by a thin layer of insulative material (the so-called buried oxide layer, or "SOI") that is sandwiched between a bulk substrate and the circuit elements of the device. Typically, no other layers of material are interposed between the SOI and the bulk substrate. In an SOI CMOS device, the circuit elements above the SOI are established by regions of a field oxide semiconductive layer which are doped as appropriate with N-type or P-type conductivity dopants. For example, for an N channel transistor, the field oxide layer will include a gate element disposed over a body region having a P-type dopant, with the body region being disposed between a source region and a drain region, each of which are doped with an N-type dopant. These devices provide an important advantage in many applications such as battery-powered mobile telephones and battery-powered laptop computers. Also, SOI CMOS devices advantageously operate at higher speeds than do bulk CMOS devices. SOI CMOS architecture eliminates inherent parasitic circuit elements in bulk CMOS due to junction capacitances between adjacent components. Also, CMOS circuits are very fast, due to the fact that the bulk capacitance is very small. SOI CMOS is also immune to latchup. Other problems surrounding the technology include the SOI floating-body effect. This particular problem has been addressed by others, by example, in a paper entitled "Suppression of the SOI Floating-body Effects by Linked-Body Device Structure," by

W. Chen, et. al., 1996 Symposium on VLSI Technology Digest of Technical Papers.

One of the obstacles facing the increased use of SOI CMOS architecture is the fact that there is an enormous economic design investment in modern VLSI integrated circuit (IC) products. Typically, standard SOI does not behave the same way as bulk CMOS because of the dielectric isolation, and bulk CMOS designs are thus generally not compatible with, or readily transferable to an SOI architecture. Product groups must decide whether to re-design circuits for SOI CMOS, even when the circuit functions adequately using bulk CMOS, especially since the fabrication facilities will not try to run any new technology without a baseline. Although the prior art teaches combination of bulk CMOS and SOI CMOS architecture, by example Chen et.al. teaches locating wells above the buried oxide layer, the prior art does not teach any layout compatibility between the two architectures nor does it teach placing wells below the buried oxide layer. Thus, a need is seen to exist to provide a SOI configuration which is compatible with current bulk CMOS architecture. Using a bulk CMOS database, it would then be possible to create products rapidly for SOI fabrication and technologies.

Accordingly, it is a primary object of the present invention to provide a method for creating a SOI CMOS type device compatible with bulk CMOS .

A related object of the present invention is to provide method for creating a SOI CMOS device compatible with bulk CMOS using a bulk CMOS physical layout data base.

Still another object of the present invention is to provide an SOI CMOS device fabricated in accordance with the foregoing objects.

SUMMARY OF THE INVENTION

According to the invention there is provided a method for creating a SOI CMOS type device compatible with bulk CMOS, which device is created using a bulk CMOS physical layout data base. The method comprises using the P-well and N-well masks used in fabrication of the bulk CMOS devices. The N-well and P-well regions are fabricated by implanting the appropriate dopants above and below the buried oxide layer to create the basic SOI CMOS structure. Particular modifications to the basic SOI CMOS structure include providing a mask for establishing ohmic contact with the wells below the buried oxide layer. This can be accomplished by the use of a separate mask

which is generated from the existing bulk CMOS mask database. The mask is generated by doing the following logical AND and OR functions on the existing CMOS layers:

a) SOURCE/DRAIN [AND] P^+ [AND] P-WELL [AND] 1st CONTACT

b) SOURCE/DRAIN [AND] N^+ [AND] N-WELL [AND] 1st CONTACT

c) a) [OR] b)

Other features of the invention are disclosed or apparent in the section entitled "BEST MODE OF CARRYING OUT THE INVENTION."

BRIEF DESCRIPTION OF THE DRAWINGS

For a fuller understanding of the present invention, reference is made to the accompanying drawings in the following detailed description of the Best Mode of Carrying Out the Invention. In the drawings:

Figure 1 is a cross-sectional view of a prior art SOI configuration.

Figure 2 is a cross-sectional view of a prior art bulk CMOS configuration.

Figure 3 is a cross-sectional view of a SOI CMOS device and architecture according to the invention.

Figure 4 is a cross-sectional view of a SOI CMOS device according to the invention, showing the well-to-substrate depletion spread and well-to-substrate capacitance.

Figure 5 shows a step in a method of forming well contact plugs in a SOI CMOS device according to the invention.

Figure 6 shows a subsequent step in the method of forming well contact plugs in a SOI CMOS device according to the invention.

Figure 7 is a cross-sectional view of a SOI CMOS device according to the invention, including well contact plugs.

Figure 8 is a cross-sectional view of a SOI CMOS device according to the invention, including well contact plugs, showing the well-to-substrate depletion spread and well-to-substrate capacitance.

Reference numbers refer to the same or equivalent parts of the present invention throughout the several figures of the drawing.

BEST MODE OF CARRYING OUT THE INVENTION

As semiconductor devices and manufacturing techniques are well known in the art, in order to avoid confusion, while enabling those skilled in the art to practice the claimed invention, this specification omits many details with respect to known items.

Figure 1 shows a conventional SOI CMOS configuration. The SOI CMOS, generally indicated by the numeral 10, comprises an N-channel MOSFET 12 and a P-channel MOSFET 14 formed above a buried silicon oxide layer 16. The buried oxide layer (BOX) 16 is formed on a silicon substrate 18. Surrounding the MOSFETs 12 and 14 is a field oxide region (FOX) 20. Each MOSFET 12, 14 includes a polycrystalline silicon gate 22. Body region 24 is P-type doped for the N channel MOSFET 12, and body region 26 is N-type doped for the P-channel MOSFET 14. As will be appreciated from Figure 1, the MOSFETs 12 and 14 are dielectrically isolated from all other MOSFETs by virtue of the BOX layer 16 and the FOX region 20, and are insulated from any conducting substrate by means of the BOX layer 16. As a result, latch-up problems are eliminated and leakage problems are minimized.

Figure 2 shows a conventional bulk CMOS configuration. The bulk CMOS, generally indicated by the numeral 30, comprises an N-channel MOSFET 32 and a P-channel MOSFET 34. The N-channel MOSFET 32 is located in a P-well 36, and the P-channel MOSFET 34 is located in an N-well 38. The P- and N-wells are formed in an N or P-type bulk 40, typically by means of ion implant and well drive. Surrounding the MOSFETs 32 and 34 is a field oxide region (FOX) 42. Each MOSFET 32, 34 includes a polycrystalline silicon gate 44.

When an electrical potential is applied to one of the gates 22 of the SOI CMOS 10, an electrical potential is drawn in the body regions 24 and 26 relative to the substrate 18. SOI MOSFET body regions have a floating electrical potential unless intentionally connected using area consuming layout methods. This effect is not found in bulk CMOS, and many bulk CMOS designs depend on the MOSFET body regions having a known electrical potential whereas SOI MOSFET's body regions are isolated from the bulk silicon. Also, circuit design simulations for SOI CMOS are based on the assumption that the MOSFETs are isolated from the bulk silicon, and circuit design performance depends on the silicon behaving in the same way as the model. Standard SOI does not behave the same way as bulk CMOS because of the dielectric isolation, and bulk CMOS designs are thus generally not compatible with, or readily transferable, to an SOI architecture.

A SOI-bulk CMOS compatible architecture according to the invention is shown in Figure 3. The SOI-bulk well CMOS, generally indicated by the numeral 50,

comprises an N-channel MOSFET 52 and a P-channel MOSFET 54 formed above a buried silicon oxide layer 56. The buried oxide layer (BOX) 56 is formed on a silicon substrate 80. Surrounding the MOSFETs 52 and 54 is a field oxide region 58 (FOX).

The N-channel MOSFET 52 includes a polycrystalline silicon gate 60, a N^+ source region 62 and a N^+ drain region 64. Between the source region 62 and the drain region 64, and below the gate 60, a P^- region 66 is provided. In Fig. 3, the source region 62 and the drain region 64 are shown to be shallower than the buried oxide layer, but in practice, the source region 62 and the drain region 64 may extend down to the buried oxide layer, as shown in Figure 4. Located below the buried oxide layer 56 and below the P^- region 66 is a region 67 which is of the same conductivity type i.e. P as the channel region 66. In the illustrated MOSFET 52, the region 67 is part of a P-well 68 which is formed above and below i.e. divided by the buried oxide layer 56. Similarly, the P-channel MOSFET 54 includes a polycrystalline silicon gate 70, a P^+ source region 72 and a P^+ drain region 74. Between the source region 72 and the drain region 74, and below the gate 70, an N^- region 76 is provided. The source region 72 and the drain region 74 are shown to be shallower than the buried oxide layer 56, but in practice, the source region 72 and the drain region 74 may extend down to the buried oxide layer 56 as shown in Figure 4. Located below the buried oxide layer 56 and below the N^- region 76 is a region 77 which is of the same conductivity type i.e. N as the channel region 76. In the illustrated MOSFET 54, the region 77 is part of an N-well 78 which is formed above and below i.e. divided by the buried oxide layer 56. It should be obvious to one skilled in the art, that other planar MOSFET designs can be applied into this well formation method e.g. gates may be metal, polycide or salicide.

By using the standard bulk CMOS P-well and N-well masks, the wells 68 and 78 are implanted both above the buried oxide layer 56 and below the buried oxide layer 56 in the bulk region. In the embodiment illustrated in Figure 3, the bulk region is an N, or P, substrate 80. One or more energy levels may be used for the ion implant of the wells 68, 78 after the buried oxide layer 56 is formed. In this regard, implant energies of 500 keV to several megavolts may be used. Alternatively, the wells 68, 78 may be formed using normal 100 keV or less implant energies followed by heavy oxygen implant for the formation of the buried oxide layer 56 using the SIMOX technique. The well drive then takes place during the oxygen implant anneal at approximately 1300□

C. The architecture in Figure 3 results in the reduction of parasitic junction capacitance under either N-channel or P-channel transistors. That is, if an N-substrate is used, the P-well will be junction isolated, that is, it will "float" electrically at approximately zero volts. A depletion zone will form between the P-well 68 and the substrate 80, which will serve to reduce charge transfer from all displacement current from electrode signals above it, eg. N^+ junctions 62, 64 and respective interconnects. The depletion zone and its effects are discussed in more detail below with reference to Figure 4.

Figure 4 shows the resistances, capacitances and the depletion zone formed under an N-channel MOSFET in the architecture according to the invention. As before, the N-channel MOSFET, generally indicated by the numeral 90 includes a polycrystalline silicon gate 92, a N^+ source region 94, and a N^+ drain region 96. Between the source region 94 and the drain region 96, and below the gate 92, a P^- body region 98 is provided. Electrical contact to the source region 94, the gate region 96 and the gate 92, is made respectively by a metal source electrode 100, a metal drain electrode 102, and a metal gate electrode 104, which penetrate through an interoxide layer 105. Also provided is a metal P-well contact electrode 106. Surrounding the various semiconductor regions below the interoxide layer 105 is a field oxide layer 107. Also as before, a buried oxide layer 108 is present below the P^- body region 98. Located below the buried oxide layer 108 and below the P^- body region 98 is a region 112, which is of the same conductivity type i.e. P as the channel region 98. In the illustrated MOSFET 90, the region 110 is part of a P- well 112 which is formed above and below i.e. divided by the buried oxide layer 108. The P-well is formed in an N type substrate 114 using a bulk CMOS P-well mask as described with reference to Figure 3. A depletion zone 116 forms between the P-well 112 and the N-substrate 114, which serves to reduce charge transfer due to displacement current induced in the substrate 114 by electrode signals applied to the N^+ regions 94, 96, and interconnect 106. Since active devices are not placed in the P-well 112, below the buried oxide layer 108, the doping levels of the P-well 112 in this region, and of the substrate 114, may be very light, less than or approximately equal to 1.0E15 atoms/cc. This results in a depletion spread i.e. the size of the depletion zone 116 of approximately 1 μm, or greater, for very lightly doped P-well/N-substrate junctions. The capacitance 118 resulting from the depletion zone 116, together with the buried oxide layer capacitance 120, which are in

series as shown, reduces the capacitance between the electrodes 100, 102, 106 and the N-substrate 114.

As discussed previously, existing bulk CMOS tooling is used in the SOI technique of the invention to form the N and P regions below the buried oxide layer shown in Figures 3 and 4. As a result, the N-channel and P-channel transistors 52, 54, and 90 are located in their respective correctly doped background material, and the substrate contacts, such as the P-substrate contact 106, will be positioned correctly to ohmically contact their underlying device wells. Thus, the SOI configuration of the invention is easily adaptable and manufacturable from existing bulk CMOS configurations, while retaining the advantages of prior art SOI configurations. It may also be desirable, in the SOI configuration of the invention, to ohmically contact the wells beneath the buried oxide layer. This can be accomplished, with some increase in process complexity, by the use of a separate mask which is generated from the existing bulk CMOS mask database. The mask is generated by doing the following logical AND and OR functions on the existing CMOS layers:

a) SOURCE/DRAIN [AND] P^+ [AND] P-WELL [AND] 1st CONTACT

b) SOURCE/DRAIN [AND] N^+ [AND] N-WELL [AND] 1st CONTACT

c) a) [OR] b)

The mask resulting from function c) is used to form a contact hole through the top silicon layer and through the buried oxide layer which may be filled with an appropriate substance for contacting the underlying wells. The formation and filling of the contact hole may be done at any step between the first step in the device fabrication process up to immediately before the N^+ or P^+ source or drain formation. In this regard, Figures 5 to 7 illustrate the formation of well contact plugs after field oxide formation.

As shown in Figure 5, after the formation of field oxide areas 130 in the silicon layer 132 above the buried oxide layer 133, a layer of photoresist 134 is deposited on the silicon layer 132. The photoresist layer 134 is exposed using the mask generated by the logical function c) above, and developed to define holes 136 in the photoresist layer 134. Then, a silicon dioxide etch is used to form the upper portions of contact holes 138 in field oxide areas 130; then a silicon etch is used to form the intermediate portions of contact holes 138. The silicon etch will normally stop on the buried oxide layer 133, and it is then necessary to switch to a plasma etch gas to etch through the buried oxide

layer 133. The plasma etch will stop on the bulk silicon (the P-well 140 or the N-substrate 142), thereby completing the formation of the contact holes 138. Since a low resistance ohmic contact is not necessary for the contact plugs, the contact plugs are formed of polycrystalline silicon (polysilicon) which is deposited onto the silicon layer 132 and into the contact plug holes 138 by means of chemical vapor deposition (CVD). The deposited polysilicon is indicated in Fig. 6 by the numeral 144. The polysilicon 144 above the silicon 132 and above the field oxide 130 is removed using chemical mechanical polishing (CMP), to leave the structure shown in Figure 7, with a polysilicon contact plug 146 penetrating the field oxide 130, the silicon layer 132 and the buried oxide layer 133 to contact the P-well 140, and a polysilicon contact plug 148 penetrating the field oxide 130, the silicon layer 132 and the buried oxide layer 133 to contact the N-substrate 142. As an alternative to polysilicon, the contact plugs 146 and 148 could be made of a refractory metal, but CVD polysilicon is preferred to eliminate contact barriers. In Figures 5 to 7, the P-well 140 is shown to be already formed. However, it is preferable to form the P-well (or N-well as the case may be) using MeV level implant energies after the formation of the contact plugs. This will result in the contact plugs having some implant doping embedded therein. This will facilitate ohmic contact through the plugs to the underlying wells. As can be seen from Figure 7, the contact plugs 146 and 148 contact the silicon layer 132 above the buried oxide layer 133, thereby also correctly contacting the respective body regions for the N- and P-channel transistors yet to be formed in Figure 7. Thus, not only is the well 140 connected to V_{ss}, but also the P-type body regions for all N-channel transistors. Likewise, not only is the N-substrate 142 connected to V_{DD}, but also the N-type body regions for all P-channel transistors.

During the subsequent N^+ and P^+ source and drain region implant, the contact plugs will receive additional doping which will improve their conductivity and further facilitate ohmic contact with the underlying wells or substrate.

It is important to note, however, that the wells below the buried oxide layer are only required to absorb reverse bias junction current leakage, and therefore, the ohmic resistance of the contact plugs may be as high as the mega-ohm range and still be acceptable. However, after undergoing the well doping and the source/drain doping as discussed above, the resistance of the plugs should be between approximately 100 ohms

and 10,000 ohms. As well, leakage current is normally 1 μA or far less, this resistance range is acceptable.

Figure 8 shows an N-channel MOSFET according to the invention, including well contact plugs, showing the well to substrate depletion spread and well to substrate capacitance.

For purposes of conciseness, common reference numerals will be used for elements which are common to Figures 4 and 8, and the discussion of these common elements above with reference to Figure 4 applies equally to Figure 8.

As can be seen from Figure 8, the MOSFET includes a polycrystalline well contact plug 150 which extends through the buried oxide layer 108 to contact the P-well 112 which underlies the buried oxide layer 108. The P-well 112 is lightly doped (less than or approximately equal to 1.0E15 atoms/cc), and is biased to the source voltage (V_{SS}) via the contact electrode 152. The substrate 114 is biased to the drain voltage (V_{DD}). The light doping and the voltage bias (V_{SS} to V_{DD}) results in a very small well-to-substrate capacitance 153, and a large (3μm to 10μm) depletion spread 154.

SOI designs claims faster gate speed than bulk CMOS. The configuration of the invention improves SOI speed further by reducing parasitic capacitance loads between the active devices and the substrate material. Further, the configuration of the invention provides the means whereby existing bulk CMOS database tooling can be used to provide a SOI configuration, with the attendant advantages inherent in SOI of reduced parasitic capacitance, improved speed, and the elimination of alpha particle SRAM memory faults. Further, by reducing the parasitic capacitance using wells implanted below the buried oxide layer, thinner buried oxide layers can be used compared to conventional SOI, reducing the large SIMOX manufacturing costs. Device yield is improved because pin-holes formed in the buried oxide layer do not affect device performance as in conventional SOI, because of the underlying wells in the configuration of the invention.

It will be appreciated that the invention is not limited to the embodiment of the invention described above, and many modifications are possible without departing from the spirit and the scope of the invention.

CLAIMS

What is claimed is:

1. A SOI CMOS device comprising:

a P-channel CMOS transistor;

an N-channel CMOS transistor;

an electrically insulating layer located below the P-channel transistor and below the N-channel CMOS transistor;

a P-type semiconductor region located below the electrically insulating layer and below the N-channel CMOS transistor; and

an N-type semiconductor region located below the electrically insulating layer and below the P-channel CMOS transistor.

2. A SOI CMOS device according to claim 1 wherein the N-type semiconductor region is a P-type substrate region.

3. A SOI CMOS device according to claim 2 wherein the P-type semiconductor region is a P-well formed in the N-type substrate region.

4. A SOI CMOS device according to claim 1 wherein the P-type semiconductor region is a P-type substrate region.

5. A SOI CMOS device according to claim 4 wherein the N-type semiconductor region is a N-well formed in the P-type substrate region.

6. A SOI CMOS device according to claim 1 wherein the N-type semiconductor region is an N-well and the P-type semiconductor region is a P-well.

7. A SOI CMOS device according to claim 6 wherein the N-well and the P-well are formed in a substrate selected from the group consisting of an undoped substrate, a P-type substrate and an N-type substrate.

8. A method of making a SOI CMOS device comprising the steps of:

providing a semiconductor substrate region;

providing a layer of electrically insulating material above the substrate region;

providing a semiconductor device region above the layer of electrically insulating material;

providing a bulk CMOS fabrication mask for forming a N-type semiconductor region in the semiconductor substrate region;

providing a bulk CMOS fabrication mask for forming a P-type semiconductor region in the semiconductor substrate region;

forming a N-type semiconductor region in the semiconductor substrate region above and below the electrically insulating layer;

forming a P-type semiconductor region in the substrate region above and below the electrically insulating layer; and

providing a P-channel CMOS transistor and an N-channel CMOS transistor in the semiconductor device region;

9. A method of making a SOI CMOS device according to claim 8 wherein the step of providing a semiconductor substrate region and the step of forming an N-type semiconductor region together comprise the step of:

providing an a N-type substrate region.

10. A method of making a SOI CMOS device according to claim 9 wherein the step of forming a P-type semiconductor region comprises the step of:

forming a P-well in the N-type substrate region.

11. A method of making a SOI CMOS device according to claim 8 wherein the step of providing a semiconductor substrate region and the step of forming a P-type semiconductor region together comprise the step of:

providing a P-type substrate region.

12. A method of making a SOI CMOS device according to claim 11 wherein the step of forming a N-type semiconductor region comprises the step of:

forming a N-well in the P-type substrate region.

13. A method of making a SOI CMOS device according to claim 8 wherein:

the step of forming an N-type semiconductor region comprises the step of forming a N-well in the semiconductor substrate region; and

the step of forming a P-type semiconductor region comprises the step of forming a P-well in the semiconductor substrate region.

14. A method of making a SOI CMOS device according to claim 13 wherein the semiconductor substrate region is selected from the group consisting of an undoped substrate, a P-type substrate and an N-type substrate.

15. A CMOS device comprising:

a first gate having a channel region which is doped to be of a first

providing a bulk CMOS fabrication mask for forming a P-type semiconductor region in the semiconductor substrate region;

forming a N-type semiconductor region in the semiconductor substrate region above and below the electrically insulating layer;

forming a P-type semiconductor region in the substrate region above and below the electrically insulating layer; and

providing a P-channel CMOS transistor and an N-channel CMOS transistor in the semiconductor device region;

9. A method of making a SOI CMOS device according to claim 8 wherein the step of providing a semiconductor substrate region and the step of forming an N-type semiconductor region together comprise the step of:

providing an a N-type substrate region.

10. A method of making a SOI CMOS device according to claim 9 wherein the step of forming a P-type semiconductor region comprises the step of:

forming a P-well in the N-type substrate region.

11. A method of making a SOI CMOS device according to claim 8 wherein the step of providing a semiconductor substrate region and the step of forming a P-type semiconductor region together comprise the step of:

providing a P-type substrate region.

12. A method of making a SOI CMOS device according to claim 11 wherein the step of forming a N-type semiconductor region comprises the step of:

forming a N-well in the P-type substrate region.

13. A method of making a SOI CMOS device according to claim 8 wherein:

the step of forming an N-type semiconductor region comprises the step of forming a N-well in the semiconductor substrate region; and

the step of forming a P-type semiconductor region comprises the step of forming a P-well in the semiconductor substrate region.

14. A method of making a SOI CMOS device according to claim 13 wherein the semiconductor substrate region is selected from the group consisting of an undoped substrate, a P-type substrate and an N-type substrate.

15. A CMOS device comprising:

a first gate having a channel region which is doped to be of a first

polarity;

a first source region which is located adjacent to the body region and which is doped to be of a second polarity which is opposite to the first polarity;

a first drain region which is located adjacent to the body region and which is doped to be of the second polarity;

an electrically insulating layer below the gate, source and body regions; and

a first semiconductor region directly below the insulating layer and below the gate, source and channel regions, the first semiconductor region being doped to be of the first polarity.

16. A CMOS device according to Claim 15 further comprising:

a second gate having a second channel region which is doped to be of the second polarity;

a second source region which is located adjacent to the second body region and which is doped to be of the first polarity;

a second drain region which is located adjacent to the second body region and which is doped to be of the first polarity;

an electrically insulating layer below the second gate, second source and second body regions; and

a second semiconductor region directly below the insulating layer and below the second gate, second source and second channel regions, the second semiconductor region being doped with to be of the second polarity.

17. A method of making a SOI CMOS device comprising the steps of:

providing a semiconductor substrate region;

providing a layer of electrically insulating material above the substrate region;

providing a semiconductor device region above the layer of electrically insulating material;

providing a first mask comprising a bulk CMOS fabrication mask for forming an N-type semiconductor region in the semiconductor substrate region;

providing a bulk CMOS fabrication mask for forming a P-type semiconductor region in the semiconductor substrate region;

forming an N-type semiconductor region in the semiconductor substrate region above and below the electrically insulating layer;

forming a P-type semiconductor region in the substrate region above and below the electrically insulating layer;

providing a second mask comprising a logical manipulation of a plurality of bulk CMOS fabrication masks, said second mask being used for forming ohmic contact with the N-type and P-type semiconductor regions formed in the semiconductor substrate region;

forming at least one ohmic contact structure contacting the N-type and P-type semiconductor regions formed in the semiconductor substrate region; and

providing a P-channel CMOS transistor and an N-channel CMOS transistor in the semiconductor device region.

18. A method of making a SOI CMOS device according to claim 17 wherein the step of providing a second mask comprises:

providing a mask created by logical manipulating of CMOS data base expressions, namely:

a) SOURCE/DRAIN [AND] P^+ [AND] P-WELL [AND] 1st CONTACT

b) SOURCE/DRAIN [AND] N^+ [AND] N-WELL [AND] 1st CONTACT

c) a) [OR] b).

19. A method of making a SOI CMOS device according to Claim 17 wherein: said step of forming at least one ohmic contact structure comprises forming ohmic contact structures for electrically contacting corresponding body region of said P-channel and N-channel CMOS transistors, as well as said N-type and P-type semiconductor regions by a source voltage.

20. A method of making a SOI CMOS device according to claim 17 wherein: said steps of forming an N-type semiconductor region and forming a P-type semiconductor region in the substrate region above and below the electrically insulating layer facilitates a step of improving device yield.

21. A method of making a SOI CMOS device according to claim 8 wherein: said steps of forming an N-type semiconductor region and forming a P-type semiconductor region in the substrate region above and below the electrically insulating layer facilitates a step of improving device yield.

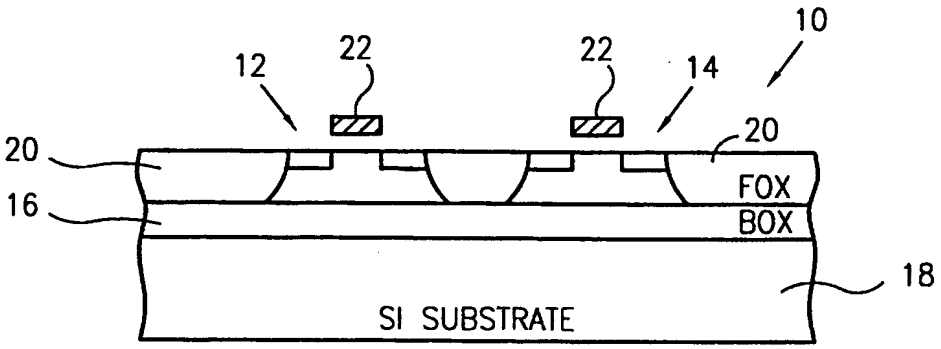

FIG. 1

(PRIOR ART)

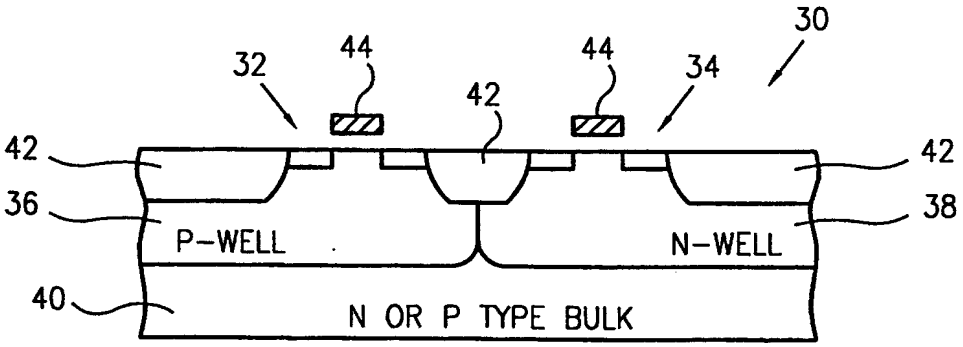

FIG. 2

(PRIOR ART)

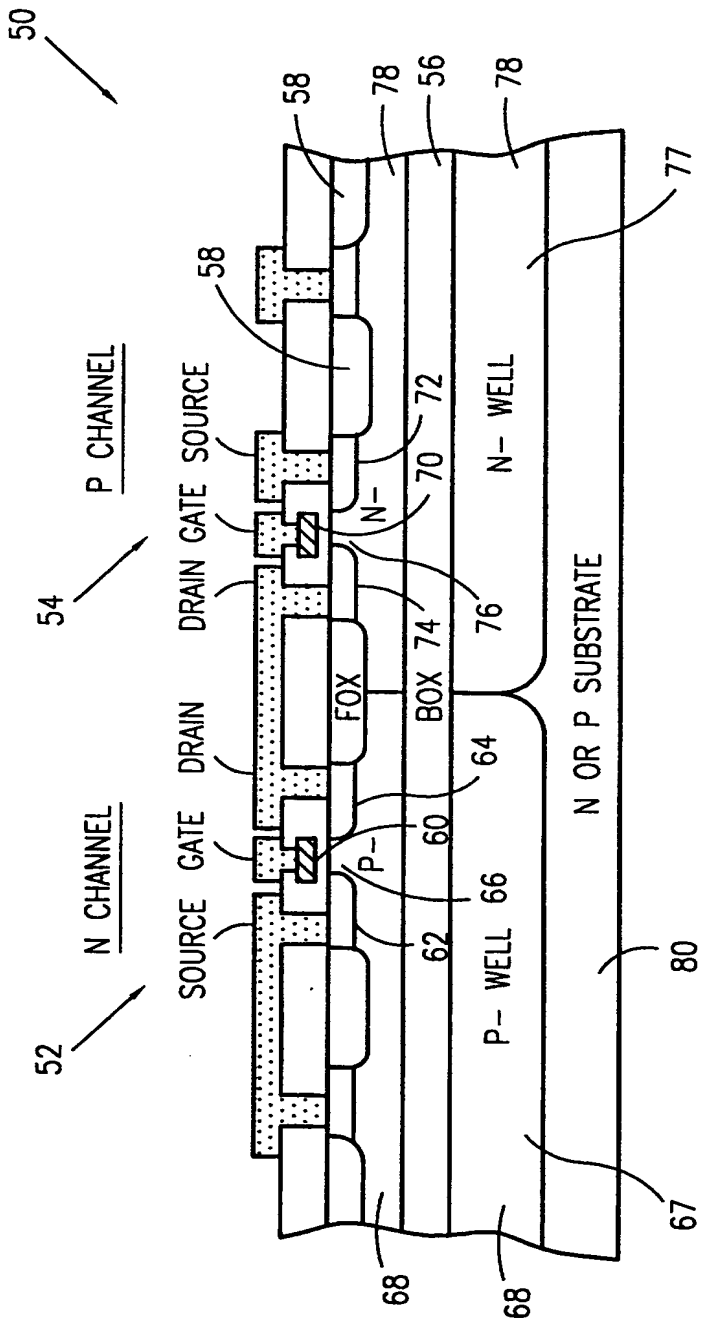

FIG. 3

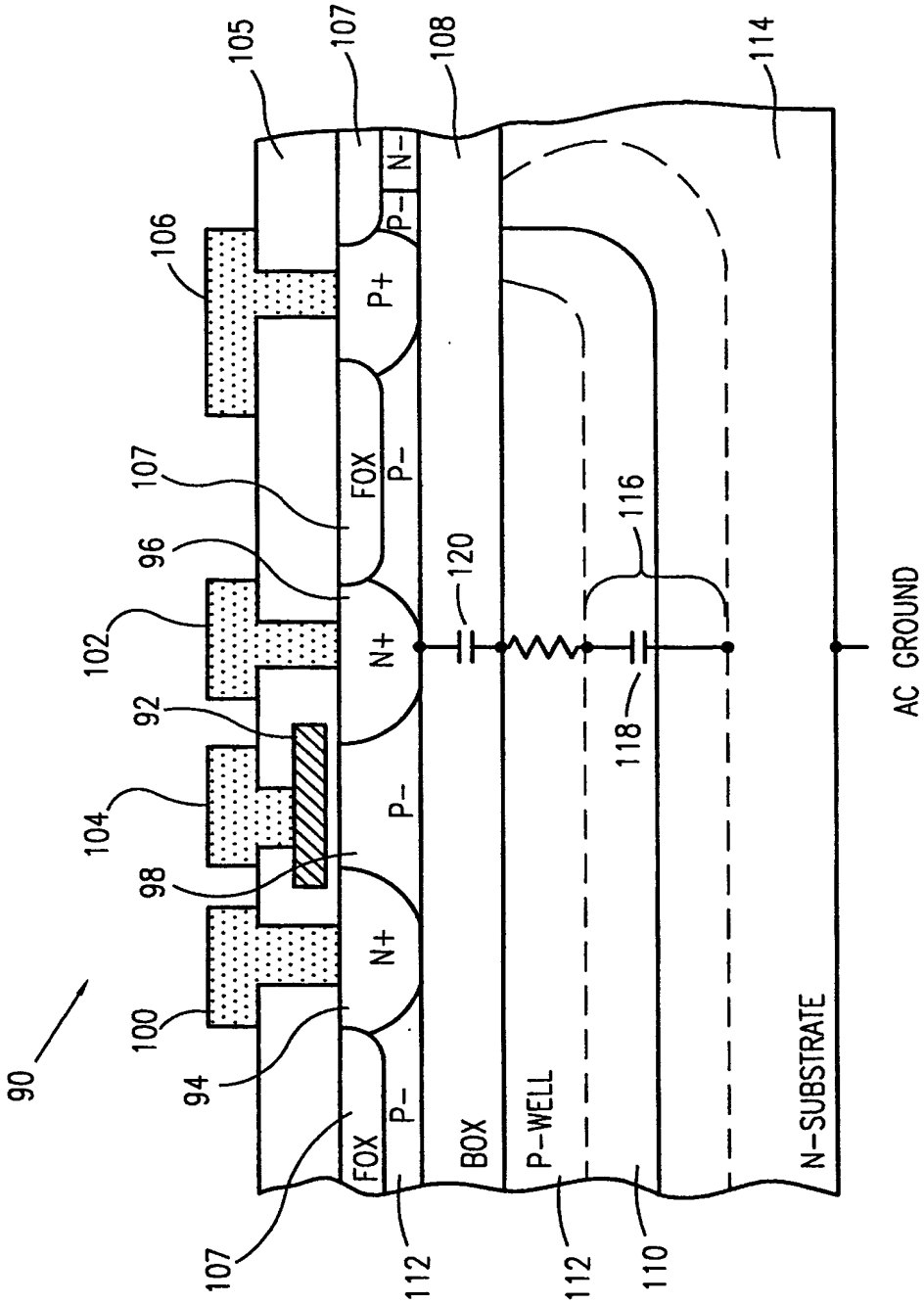

FIG. 4

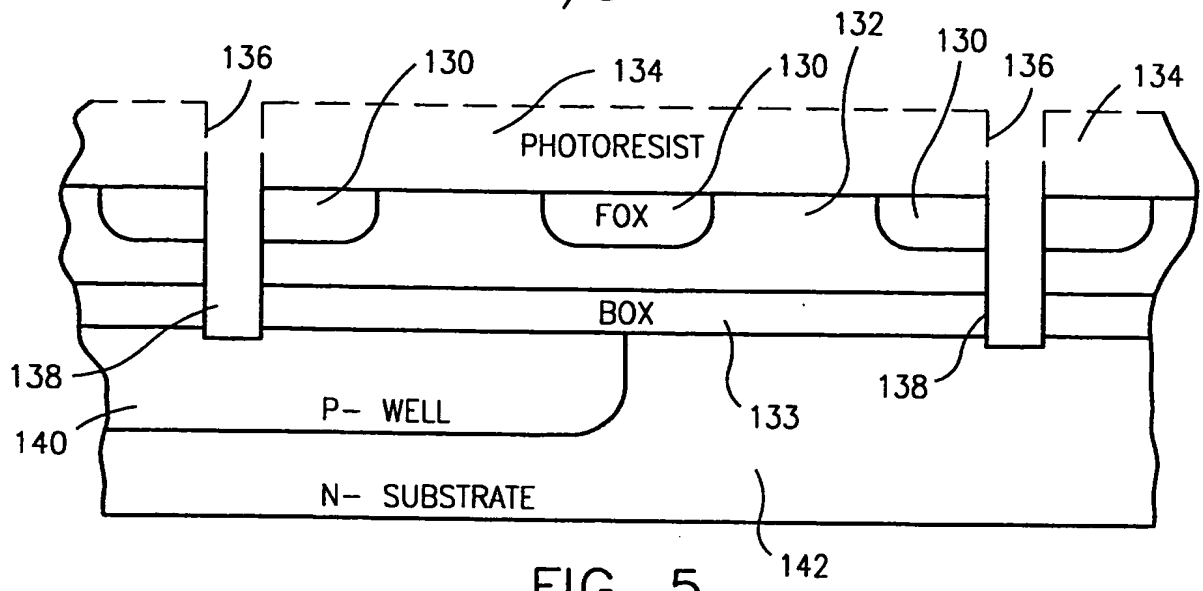

FIG. 5

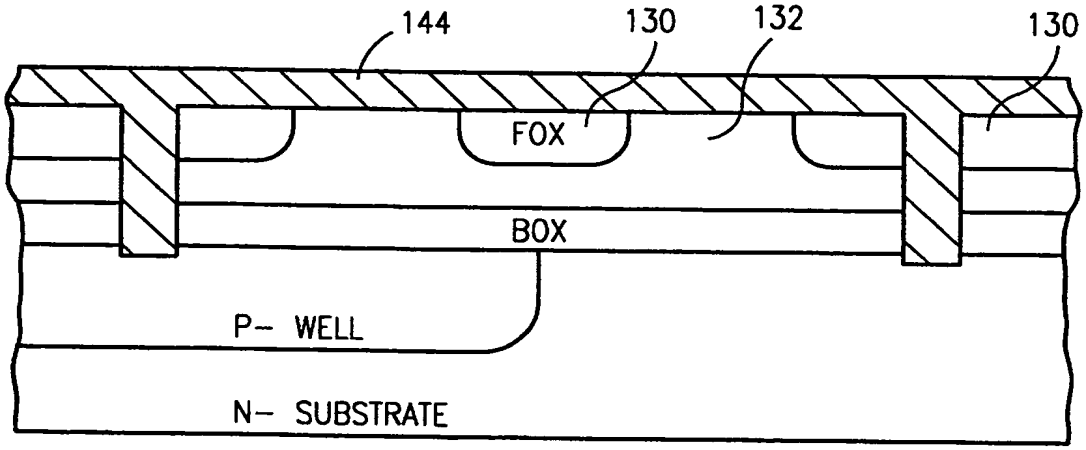

FIG. 6

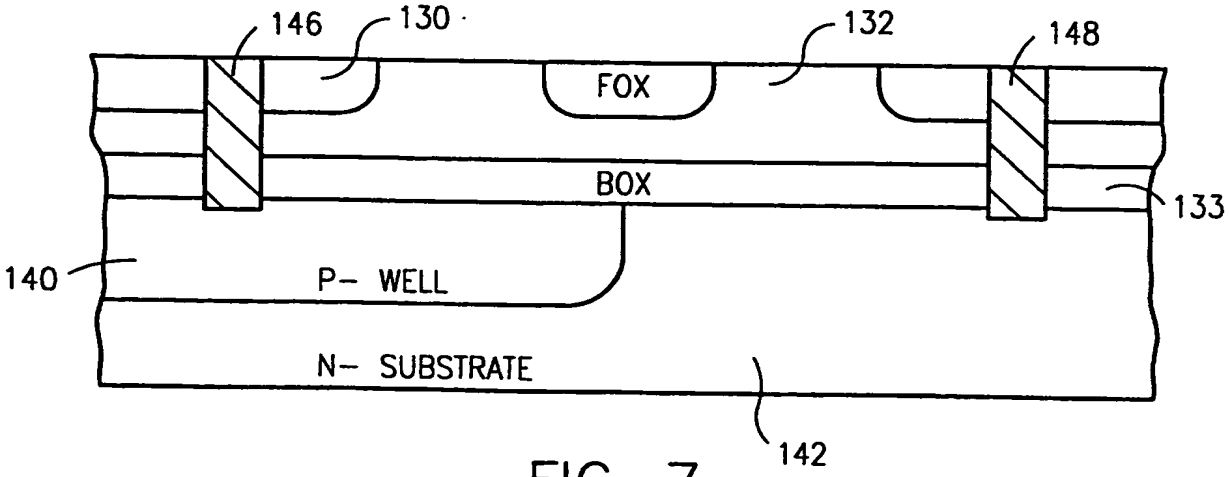

FIG. 7

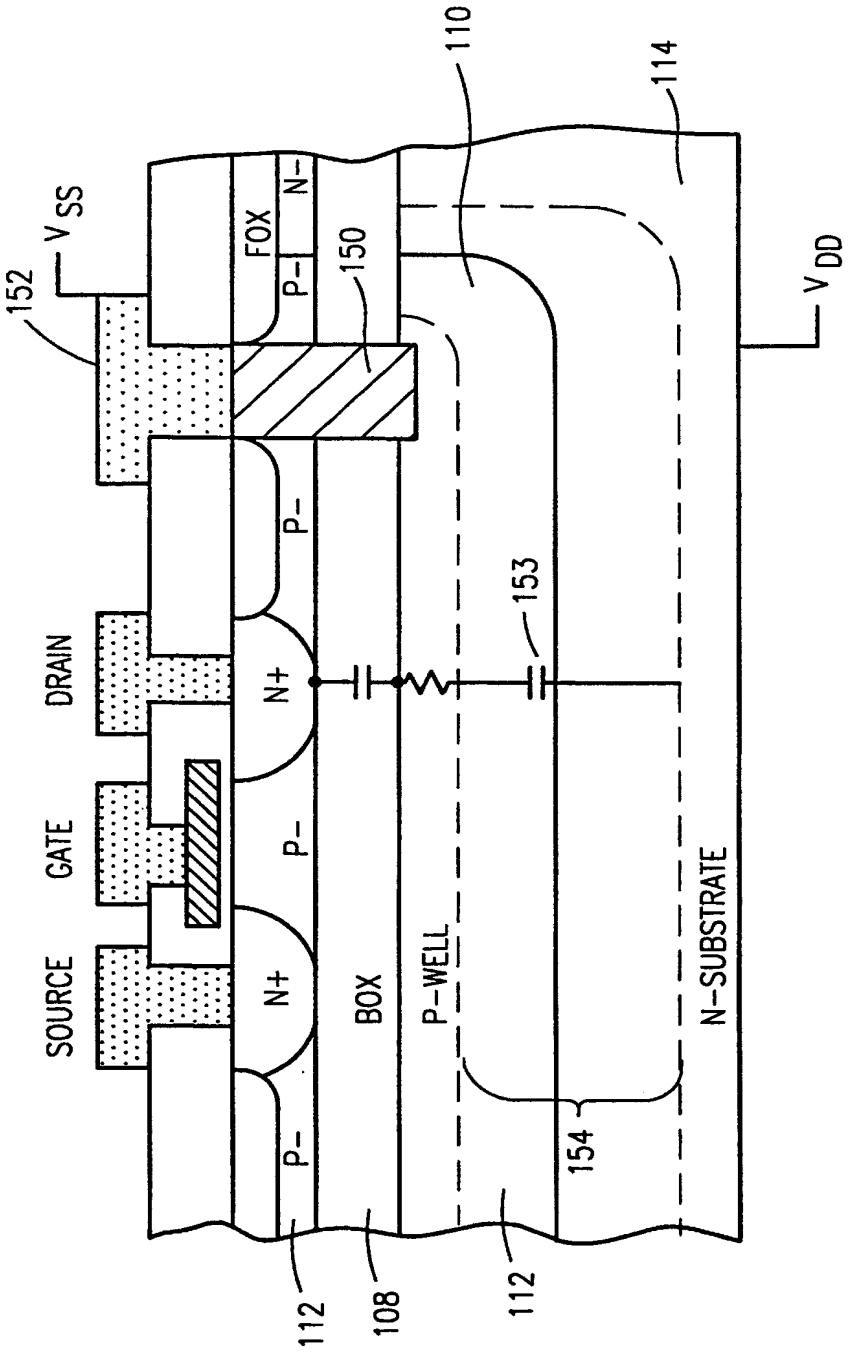

FIG. 8

INTERNATIONAL SEARCH REPORT

International Application No
PCT/US 98/26846

A. CLASSIFICATION OF SUBJECT MATTER
IPC 6 H01L27/12 H01L21/84

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 6 H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	EP 0 694 977 A (NIPPON ELECTRIC CO) 31 January 1996	1-5, 8-12, 15-21
A	see page 10, column 15, line 14 - page 13, column 21, line 39; figures 30-41N	6,7,13, 14
X	US 5 359 219 A (HWANG JEONG-MO) 25 October 1994	1,6-8, 13-16,21
A	see column 2, line 34 - column 4, line 39; figures 1A-G	2-5, 9-12,17, 18,20

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[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

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"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

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"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
16 April 1999	26/04/1999

Name and mailing address of the ISA	Authorized officer
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1

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INTERNATIONAL SEARCH REPORT

International Application No
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C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication,where appropriate, of the relevant passages	Relevant to claim No.
X	YOSHINO A ET AL: "HIGH-SPEED PERFORMANCE OF 0.35 MUM CMOS GATES FABRICATED ON LOW-DOSE SIMOC SUBSTRATES WITH/WITHOUT AN N-WELL UNDERNEATH THE BURIED OXIDE LAYER" IEEE ELECTRON DEVICE LETTERS, vol. 17, no. 3, 1 March 1996, pages 106-108, XP000584745	1-5, 8-12, 15-21
A	see page 106, column 1, line 1 - column 2, line 30; figure 1	6,7,13, 14

1

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INTERNATIONAL SEARCH REPORT

Information on patent family members

International Application No
PCT/US 98/26846

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
EP 0694977 A	31-01-1996	JP 8032040 A	02-02-1996
US 5359219 A	25-10-1994	US 5426062 A	20-06-1995